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for

A DELAY LOCK LOOP CIRCUIT USEFUL IN A SYNCHRONOUS SYSTEM  
AND ASSOCIATED METHODS

by

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## BACKGROUND

The present invention relates to computer systems having synchronous data transfer interfaces and also to synchronous memory devices that interface with a synchronous data bus. More particularly, the present invention relates to a delay lock loop of a synchronous memory that comprises an initialization circuit for initializing the delay lock loop to a stable and reliable operating condition.

Known prior art computer systems include processors that exchange data with a variety of memory and input/output peripheral devices. Exemplary memory devices include read only memory (ROM), dynamic random access memory (DRAM), and/or static random access memory (SRAM). Exemplary input/output peripheral devices may include a keyboard, mouse, printer or video display unit. These exemplary memory and peripheral devices typically exchange data with a processor by way of a data bus.

Synchronous dynamic random access memories (SDRAMs) employ pipelined data transfers to a processor or bus for effecting data transfer rates that are comparable to the processor's operating frequency. However, because the processor's operating frequency might be different from that of the SDRAM, a memory controller may be required between the SDRAM and the processor for accommodating their different operating speeds.

Synch-link DRAM (SLDRAM), another known type of memory, exchanges data in packet formats, wherein packets of data are sent or received, as determined in accordance with a received command packet, directly to or from a processor and in synchronous relationship thereto. Additionally, if communicating directly with a processor, the SLDRAM may not require an intermediate memory controller.

In accordance with one such exemplary prior art SLDRAM system architecture, and method of operation, a master clock propagates from a processor to a plurality of SLDRAMs to assist system synchronization, with an aim of facilitating synchronous transfer of data between the processor and memory devices. As a part of this synchronization scheme, the master clock might be used to provide the basis for the generation or correlation of signals within the SLDRAM.

With reference to Figures 1 and 2, an exemplary, prior art SLDRAM, hereinafter memory 10, is coupled to a bus 12. Memory 10 includes an output latch 14 and buffer 15. Data is sent from these devices to bus 12 via output terminal 21. The memory also sends a clock signal,

1 which corresponds to that which was used to capture data within latch 14, to a terminal 23 via  
2 delay element 13 and buffer 16. The output clock signal is provided to facilitate the transfer of  
3 data across bus 12 to other devices, e.g., such as a processor. Ideally, for these signals that are  
4 output from the memory's output terminals, and referencing the waveforms of Figure 2,  
5 transitions 32 of the data signal 28 coincide with the rising or falling edges 34 of the clock signal  
6 30.

7 A synchronous relationship is also desired for a data signal and an accompanying clock  
8 signal when writing into the memory. Referencing Figures 3 and 4, a memory 10 is coupled to  
9 bus 12, which bus comprises N data lines 24 and M clock lines 26. Terminal 39 of memory 10  
10 receives a data signal (e.g., waveform 43 of Fig. 4), which data signal is internally coupled to the  
11 data input of latch 33. Terminal 45 receives a clock signal (waveform 42 of Fig. 4) that is  
12 forwarded to the clock input 36 of data latch 33 by way of delay unit 35. Preferably, delay unit  
13 35 provides an amount of delay  $T_{d1}$  that appropriately positions a rising edge of the delayed  
14 clock signal 44 to a time placement  $t_1$ , relative the data signal, which time placement is  
15 coincident with the center of the data eye of the data signal 43 received at the data input of latch  
16 33. However, the amount of delay that is required for optimal placement of the clock edge may  
17 change dependent upon design parameters of the data latch 33, such as its input capacitance, and  
18 any RC time constants associated with the delay circuit 35. In addition, the memory's supply  
19 voltage and its operating temperature can affect the desired optimal placement of the clock edge.  
20 Further pushing these synchronization needs, increases in computer speeds are making the  
21 processing systems less tolerable of timing changes that might be effected by voltage or  
22 temperature variations. Accordingly, delay lock loops and associated vernier circuits have been  
23 used to attempt calibration, adjustment and/or compensation of these timing changes that occur  
24 over a circuit's lifetime.

25 A known exemplary delay lock loop is shown as a part of memory 10 in Figure 5.  
26 Memory 10 receives command data from data lines 24 of bus 12, at terminals 39A via command  
27 data lines 38A. Write data is received at terminal 39B via lines 38B. A system clock of clock  
28 lines 26, is received at terminal 41 by way of line 40, while the clock signal associated with the  
29 synchronous write data transfer is received at terminal 45 via line 46. The command data that is  
30 received at terminal 39A is forwarded to the data input of command latch 66 after passing  
31 through buffers 65. A command clock is presented to the latch input of command latch 66 by

1 way of a previously programmed vernier select circuit 64. Vernier select circuit 64 comprises  
2 vernier 60 and multiplexer 62. Vernier 60 receives the command clock and provides a plurality  
3 of variously delayed representations of the command clock at the CCLK1-CCLKN outputs.  
4 Having been previously programmed in a known fashion, multiplexer 62 selects a particularly  
5 delayed representation of the clock signal for selecting an edge placement of the selected delayed  
6 clock signal that is to be substantially coincident with centers of eye patterns of the data signal  
7 received at the data input of latch 66. This delayed clock signal, which selection is routed by  
8 multiplexer 62, is forwarded as the latching clock signal to the command latch 66 for use in  
9 capturing the command data therein.

10 A signal from one of the outputs of vernier A, typically the output of greatest delay, e.g.,  
11 CCLKN, is fed back as the variably delayed signal of the delay lock loop to variable input 70 of  
12 phase detector 72. The phase detector 72 compares the phase of the signal at variable input 70 to  
13 that of the reference signal received at reference input 74. The reference signal corresponds to  
14 the received system clock, but delayed by an amount associated with the propagation delay of  
15 buffer 73. Phase detector 72 generates an error signal at its output 75 in accordance with the  
16 detected phase difference between the variably delayed signal and the reference signal. Integrator  
17 76 receives the error signal from phase detector 72 and generates a tune voltage (V<sub>tune</sub>) by  
18 integrating the error signal. The tune voltage from the integrator is coupled to the control input of  
19 vernier A and is used for adjusting the amount of delay that is provided by vernier A. Upon  
20 acquiring a locked condition, the delay lock loop aims to keep the phase of the variably delayed  
21 signal at variable input 70 coincident with that of the reference clock. Thus, the delay lock loop  
22 strives to preserve the integrity of data reception by, ideally, keeping a latching edge of the  
23 selected, vernier-delayed clock signal centered within the data eye of the data signal that is  
24 received at the data input of latch 66.

25 When channeling command data to memory 10, the external system, e.g., a processor,  
26 supplies a continuous system clock on line 40, which runs continuously over time. On the other  
27 hand, when transferring write data that is to be written into the memory device, the clock that  
28 accompanies the write data on line 46 may be discontinuous, i.e., present only for a duration for  
29 accompanying the data transfer. Because the accompanying data clock is not continuous, a  
30 separate "slaved" vernier circuit 48 is configured for selecting optimally delayed representations  
31 of the data clock for latching data into respective registers of the receiving write data latches 33.

1 “Slaved” vernier 48 receives the tune voltage that is generated by the continuously locked delay  
2 lock loop associated with receiving the command data. This configuration assumes, of course,  
3 that the circuitry of vernier 48 and multiplexer 52 correspond to that of vernier 60 and  
4 multiplexer 62, and that any variations with respect to voltage and temperature experienced in  
5 one will correspond substantially to that experienced by the other. Accordingly, the tune voltage  
6 adjustments generated for the one, preferably, is able to, likewise, sufficiently compensate the  
7 other for keeping the intermittent data clock appropriately positioned relative to its write data  
8 signal.

9 Control logic 58, as known in the art, establishes the configurations of multiplexers 52,  
10 62 and controls operation of access circuitry 54 associated with accessing memory array 56.

11 To summarize, the control loop associated with the exemplary delay locked loop of  
12 Figure 5 includes the variable input 70 of phase detector 72, integrator 76, the control input 77A  
13 of vernier A 60, and the return line to the variable input 70. It is noted, however, that for this  
14 exemplary prior art embodiment, multiplexer 62 resides outside the control loop of the delay  
15 lock loop. Accordingly, changes in the multiplexer’s operating temperature or voltage might  
16 affect its propagation delay, and likewise might adversely impact the placement of the clock  
17 signal relative to the data signal.

18 Addressing this short coming of the multiplexer, and referring to Figure 6, the prior art  
19 provided the “compound” delay lock loop. Essentially, the compound delay lock loop comprises  
20 an outer delay lock loop wrapped around an inner delay lock loop. For the exemplary compound  
21 delay lock loop of Figure 6, the outer delay lock loop comprises phase detector 72B, integrator  
22 76B,  $V_{\text{tuneB}}$  control input 79, variable delay 98, the 180° signal path through vernier 60 (i.e.,  
23 relative to the first tap  $T\phi$ ), emulator circuit 88 and the return back to the variable input 70 of  
24 phase detector 72B. The emulator circuit 88 incorporates emulating multiplexer 90 and  
25 emulating driver 92 for emulating the delay characteristics of external multiplexer 62 and driver  
26 61 that are external the control loop of the delay lock loop. Having the emulator circuit within  
27 the control loop allows the delay lock loop to substantially compensate for deviations of the  
28 external elements (e.g., multiplexer 62 and driver 61) by way of the delay lock loop  
29 compensating the variations of surrogate emulator circuit 88.

30 If the delay of the emulator circuit changes, as may be effected by a voltage or  
31 temperature change, the phase detector 72B detects a phase difference between the variable

1 signal at variable input 70 and the reference clock at the reference input 74, and an error signal to  
2 integrator 76B responsive to the detected phase difference is generated. Depending on the  
3 direction of the phase shift, integrator 76B will ramp the tune voltage  $V_{\text{tuneB}}$  up or down for  
4 adjusting the delay of variable delay element 98 with an aim for compensating the change in  
5 delay of the emulator circuit. For example, if the delay through the emulator circuit 88 should  
6 increase, then the control loop of the delay lock loop will attempt to decrease the delay of the  
7 variable delay element 98 to keep the phase of the variable signal substantially coincident (or  
8 "locked") to that of the reference signal at the reference input 74. Likewise, if the delay through  
9 the emulator 88 should decrease, then the delay lock loop will increase the delay of the variable  
10 delay element 98.

11 Provided that emulator circuit 88 accurately emulates the external multiplexer 62 and  
12 driver 61 per their delay sensitivities with respect to voltage and temperature, then the outer  
13 loop's control of the variable delay element keeps the latching transitions of the signal at the  
14 latching input of latch 66 substantially optimally positioned, thereby substantially  
15 accommodating temperature- or voltage-effected delay variations of multiplexer 62 or buffer 61.

16 The inner delay locked loop, further referencing Figure 6, comprises multi-tap vernier 60,  
17 phase detector 72A and feedback circuit 76A. The feedback circuit has its output coupled to the  
18 control input 77A of vernier 60 and provides the tune voltage  $V_{\text{tuneA}}$  for controlling the vernier's  
19 delay. When locked, the inner delay lock loop maintains the relative phase relationships of the  
20 variously delayed signals of the vernier's output taps, with an aim of accommodating any  
21 temperature or voltage changes that might otherwise affect vernier 60. More particularly, the  
22 inner delay lock loop ideally provides a control signal  $V_{\text{tuneA}}$  to the control input 77A of vernier  
23 60 for maintaining a  $180^\circ$  phase difference between the signals of the vernier's first and last  
24 output taps.

25 In operation, referencing the timing diagrams of Figure 7, a system clock (CMDCLK)  
26 passes through buffer 73 (of Fig. 6) to provide signal A. Variable delay element 98 provides  
27 signal B with a delay determined in accordance with the value of the outer loop's control signal  
28  $V_{\text{tuneB}}$ . Vernier 60 receives signal B and outputs progressively delayed representations C, D, etc.,  
29 of signal B at taps T0, T1. . . T15. The incremental delay between the output taps may be, in  
30 general, equal to the vernier's total delay divided by the number of taps. The inner delay lock

1 loop controls the delay of vernier 60 by providing a value for control signal  $V_{\text{tuneA}}$  for  
2 maintaining a  $180^\circ$  phase difference between signals C and D of the first and last taps.

3 As determined by the configuration signals 63, multiplexer 62 selects desired output taps  
4 of vernier 60 from which to source different internal signals of the memory. For example, the  
5 configuration signal  $Y1SEL<0:3>$  for a first channel configures the multiplexer to select a  
6 particular one of the 16 taps from which to source the command clock signal E for driving the  
7 latch input of command latch 66. Likewise, the configuration signal  $Y2SEL<0:3>$  determines the  
8 tap from which to source another clock signal F. Known calibration procedures obtain values for  
9 the configuration signals, which are determined to obtain the optimally delayed representations  
10 of the system clock for their respective application. For the application associated with the  
11 command clock signal E, the calibrated value for configuration signal  $Y1SEL<0:3>$  obtains an  
12 optimally delayed representation of the system clock for placing a rising edge of the derived  
13 signal E centered within (relative to) a data eye of the data signal H as received by latch 66.  
14 Similarly as discussed relative to Figure 5, command data buffer 65 and command clock buffer  
15 73 are designed similarly to provide similar propagation delays with similar temperature or  
16 voltage sensitivity characteristics, as portrayed by the waveforms A and H relative to CMDCLK  
17 and CMDDATA.

18 Further referencing Figure 6, and as already noted, the compound delay locked loop  
19 provides the command clock for latching command data into latch 66. Emulator circuitry 88  
20 simulates multiplexer 62 and clock driver 61 so that the outer delay lock loop can adjust the  
21 delay of the variable delay element 98 for accommodating the delay deviations of the emulated  
22 external elements to present an optimal timing relationship of the command clock signal relative  
23 to the data signal received by latch 66. In other applications, such as, for example, writing data  
24 from the memory to a bus or receiving data to be written within the memory, the delay lock loop  
25 may need to accommodate delay changes effected by voltage or temperature sensitivity  
26 characteristics of, e.g., an output driver, edge shaper, or other signal conditioning circuit.  
27 However, with the prior art delay lock loops discussed herein, the emulator circuit for emulating  
28 the multiplexer, driver, shaper and/or other conditioning circuits, because of temperature or  
29 voltage variations, may accumulate, a delay shift magnitude that exceeds an adjustment limit of  
30 variable delay element 98. This is especially true if the delay lock loop was initialized with the

1 variable delay element set near its lower limit. Accordingly, the memory's data transfer integrity  
2 can be compromised.

3 To better appreciate the problems of the prior art, one should note that a delay lock loop  
4 can lock with a delay that is an integral number of clock cycles long, i.e., the delay may be 1, 2,  
5 3, or more cycles of the input frequency. Referring to Figure 6, the problem to be solved arises  
6 when the delay between nodes B and G is slightly less than an integral number of clock cycles.  
7 The loop may lock with the delay of variable delay element 98 near the minimum of its range. If  
8 the temperature or supply voltage causes the delay of emulator circuit 88 to increase, variable  
9 delay 98 will then be unable to decrease, causing the loop to unlock. One solution to this  
10 problem is to run the loop at a submultiple of the clock frequency by inserting a frequency  
11 divider directly following buffer 73, and choosing the divisor such that the delay between nodes  
12 B and G is substantially less than one cycle of the divided clock. However, even with a  
13 frequency divider, a problem can also occur if the loop locks with the delay of variable delay 98  
14 near the maximum of its range. A decrease in the delay of emulator circuit 88 will again cause  
15 the loop to unlock.

16 Accordingly, there exists a need to assure the integrity of data transfer for synchronous  
17 data networks and its associated synchronous memory. Additionally, there exists a need to  
18 improve the reliability and initialization of delay locked loops of such synchronous memory. The  
19 present invention recognizes these needs and proposes solutions thereto.



## SUMMARY OF THE INVENTION

A method and circuitry for a delay lock loop useful in synchronizing the accessing of a memory array with a system clock is disclosed. In a preferred embodiment, the delay lock loop includes a variable delay element. The delay of the variable delay element is initially set to a minimum delay value. The system clock is then frequency divided and sent to the variable delay element, the output of which will ultimately be used to access the memory array in a synchronized manner with the system clock. The frequency divided clock and the output of the variable delay element are input to a phase detector, which creates a control signal for adjusting the delay of the variable delay element. After the signals are determined to be locked by the phase detector, an undivided clock signal version of the clock signal is sent to the variable delay element, and a frequency divided version of the output of the variable delay element is sent to the phase detector in lieu of the previous output of the variable delay element.

## BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will be understood from reading descriptions of particular embodiments with reference to specific embodiments illustrated in the appended drawings. These drawings depict only exemplary embodiments of the invention and are not therefore to be considered limiting of its scope.

Figure 1 is a simplified schematic diagram of an exemplary prior art synchronous memory device.

Figure 2 is a simplified timing diagram illustrating signals associated with sending data out of a memory device.

Figure 3 is a simplified schematic diagram representative of an exemplary prior art synchronous memory device coupled to a bus for receiving data.

Figure 4 is a timing diagram illustrating signals associated with receiving data.

Figure 5 is a schematic diagram representative of a prior art synchronous memory device incorporating circuitry for receiving command data and circuitry for receiving write data.

Figure 6 is a schematic diagram representative of a prior art compound delay lock loop.

Figure 7 is a timing diagram of various signals during operation of the circuit of Figure 6.

1        Figure 8 is a simplified block diagram of a delay lock loop with initialization circuitry in  
2        accordance with an exemplary embodiment of the present invention.

3        Figures 9A-9B provide a simplified block diagram of a compound delay lock loop of  
4        another exemplary embodiment of the present invention.

5        Figure 10 is a more detailed schematic diagram for a particular exemplary embodiment of  
6        the compound delay lock loop of Figures 9A-9B.

7        Figure 11 is a timing diagram showing a sequence of signals during operation of a delay  
8        lock loop of an exemplary embodiment of the present invention.

9        Figure 12 is a schematic diagram of an exemplary divider and a multiplexer for the  
10       circuit A of Figure 10.

11       Figure 13 is a schematic diagram of an exemplary divider and a multiplexer for the  
12       circuit B of Figure 10.

13       Figure 14 is a block diagram for an exemplary phase detector and charge pump.

14       Figure 15 is a schematic diagram of an exemplary phase detector circuit.

15       Figure 16A is a timing diagram characterizing operation of the phase detector and charge  
16       pump of Figure 14 when the variable and reference clock signals are coincident with one  
17       another.

18       Figure 16B is a timing diagram characterizing operation of the phase detector and charge  
19       pump of Figure 14 when the phase of the variable signal leads that of the reference clock.

20       Figure 16C is a timing diagram characterizing operation of the phase detector and charge  
21       pump of Figure 14 when the phase of the variable signal at the phase detector lags that of the  
22       reference clock input.

23       Figure 17 is a schematic diagram of an exemplary charge pump.

24       Figure 18 is a schematic diagram of an exemplary lock sequencer for initializing a delay  
25       lock loop pursuant to an exemplary embodiment of the present invention.

26       Figure 19 is a schematic diagram of an exemplary voltage clamp circuit for clamping a  
27       control signal during an initialization sequence of an exemplary embodiment of the present  
28       invention.

29       Figure 20 is a simplified block diagram representative of a synchronous memory device,  
30       incorporating read and write data circuitry in accordance with an exemplary embodiment of the  
31       present invention.

1        Figure 21 is a simplified block diagram representative of a synchronous memory device,  
2        incorporating a clock initialization and synchronization circuit for a write channel of the  
3        synchronous memory device in accordance with an exemplary embodiment of the present  
4        invention.

5        Figure 22 is a block diagram of a computer system coupled to a synchronous network in  
6        accordance with an exemplary embodiment of the present invention.

## 8                    **DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS**

9        The present invention generally relates to synchronous memories and to delay lock loops  
10       for such synchronous memories that incorporate initialization circuitry for initializing a delay  
11       lock loop within a stable and reliable configuration.

12       To briefly summarize the disclosed solution to the problems presented by the prior art,  
13       and referring again to Figure 6, the delay lock loop is initialized with the delay of variable delay  
14       98 at its minimum, while also incorporating circuitry that assures that the delay of 98 slews in a  
15       positive direction until the loop locks. As will be seen, frequency dividers are useful in  
16       achieving this result. However, the disclosed solution requires that the desired frequency at the  
17       variable input 70 of phase detector 72B is the divided clock, while the desired frequency from  
18       clock drivers 61 and simulated clock driver 92 is the undivided clock. Accordingly, the loop is  
19       initialized with the divider for the variable path positioned ahead of variable delay 98, and then  
20       after the loop is stabilized, the location of the divider is switched such that it is inserted between  
21       simulated clock driver 92 and variable input 70 of the phase detector 72B. The divider between  
22       buffer 73 and reference input 74 of phase detector 72B remains fixed. The details of the solution  
23       follow.

24       Referencing Figure 8, a delay lock loop 140 in accordance with an exemplary  
25       embodiment of the present invention comprises a clock input 141 coupled to frequency divider  
26       142 and also to a first terminal of switch 150. The output of divider 142 is coupled to the second  
27       terminal of switch 150. Switch 150 selectively couples variable delay element 144 to receive  
28       either the divided clock signal via divider 142, or the undivided clock signal directly from input  
29       141. Control line 170 provides a control signal to switch 150 to determine its configuration. The  
30       variable delay element 144 provides a propagation delay that is determined in accordance with  
31       the value of a control signal  $V_{tune}$  that is received at its control input 166. In accordance with an

1 exemplary embodiment of the present invention, variable delay element comprises an adjustable  
2 propagation delay between minimum and maximum nanoseconds, which may vary upon the  
3 application at hand and the clock speed.

4 An optional aspect of the preferred embodiment comprises a duty cycle compensator 181  
5 disposed in the signal path between switch 150 and variable delay element 144. The duty cycle  
6 compensator 181 will condition an asymmetric input signal, for example, one having a longer  
7 high duration versus the low duration to provide a symmetrical output signal of the same  
8 frequency. U.S. patent application serial number 09/654,226 filed 8/30/2000, assigned to the  
9 assignee of the present application, and hereby incorporated by reference in its entirety, discloses  
10 exemplary embodiments and operation of such a duty cycle compensator 181.

11 The output of divider 142 is also coupled to the reference input 155 of phase detector  
12 154. This signal path to the phase detector 154 does not require a duty cycle compensator  
13 because this is unnecessary given the operating principles of divider 142. This is because the  
14 divider 142 acts upon either the rising or falling transitions of the signal at its input.  
15 Accordingly, and assuming a periodic input signal, the resulting divided output signal is  
16 symmetric.

17 Returning to the signal path associated with the variable delay, the output of variable  
18 delay element 144 is coupled to the input of delay block 146. As is well known in the art, delay  
19 block 146 includes circuits for conditioning the clock signal prior its presentation at destination  
20 terminal 147. Exemplary conditioning circuits include an output buffer, a shaping or sharpening  
21 circuit, and/or other circuits for providing sufficient output current or sharpness for the output  
22 signal to drive one or more latch inputs within the memory. For example, the output clock signal  
23 may need sufficient sharpness and current for driving a long signal line within the memory  
24 device, or, alternatively, for driving a signal line to accompany a synchronous data transmission  
25 external to the memory. Regardless of the specific application, such conditioning circuits of  
26 delay block 146 will delay the clock signal before reaching destination 147.

27 With the conditioning circuits within the control loop of the delay lock loop, delay lock  
28 loop 140 is able to control the timing relationship of the clock signal presented to destination 147  
29 such that the output clock is substantially synchronous and coincident with the reference signal at  
30 the reference input 155 of phase detector 154. For an alternative configuration that incorporates  
31 delay unit 174, the output clock is made synchronous and coincident to the clock at input 141.

1 These operating principals of the delay lock loop will become more apparent as further details  
2 are explained below.

3 Further referencing Figure 8, second divider 148 receives and frequency divides the  
4 output signal of delay 146 to provide a divided output signal to a first select terminal of switch  
5 152. The second select terminal of switch 152 receives the undivided signal directly from delay  
6 146, by way of an alternative path that bypasses divider 148. In accordance with an alternative  
7 aspect of this embodiment, an optional delay unit 174 is serially disposed within the bypass path  
8 and provides a delay comparable to that of divider 148. This assures that transitions of the clock  
9 signal as presented to the second select terminal of switch 152 are substantially coincident with  
10 the output transitions as would otherwise be provided by divider 148. This coincident timing  
11 configuration allows system transients or jitter during operation of delay lock loop 140 to be  
12 minimized when switch 152 is switched from a first position to its second position.

13 The output terminal of the switch 152 is coupled to the variable input 153 of phase  
14 detector 154. The variable input 153 of phase detector 154 is termed "variable" because of its  
15 association with variable delay element 144. The reference input 155 of phase detector 154 is  
16 electrically coupled to receive a signal from the output of first divider 142. When the delay lock  
17 loop is locked and stabilized, the phase of the signal arriving at the variable input 153  
18 corresponds to that of the signal arriving at reference input 155. Therefore, if temperature or  
19 voltage variations change the delay of block 146, phase detector 154 will determine a phase  
20 difference and provide an error signal responsive to the determined phase difference. Assuming  
21 that switch 160 is closed, integrating capacitor 158 accumulates charge from charge pump 156  
22 for providing control signal  $V_{tune}$ . As a result, the control signal  $V_{tune}$  will ramp up or down,  
23 depending upon the determined phase error, for adjusting the delay of variable delay element 144  
24 for absorbing the delay fluctuation of delay block 146. As a result, clock transitions at  
25 destination 147 are kept coincident with transitions of the reference clock input 141.

26 In normal operation, the first switch 150 of the delay lock loop 140 couples the clock  
27 input directly to the variable delay element 144, while the second switch 152 couples the second  
28 divider 148 to the variable input 153 of phase detector 154. Switch 160 is closed for coupling the  
29 charge pump to integrating capacitor 158, and switch 164 opened for disconnecting the control  
30 input 166 from the clamp voltage  $V_{min}$ . Ideally, variable delay element 144 establishes a  
31 propagation delay sufficient for synchronizing a rising edge of a clock transition at the variable

1 input 153 to a transition of the clock received at the reference input 155. Accordingly, should  
2 delay block 146 experience an increase in propagation delay, for example, due to temperature or  
3 voltage changes, then the delay lock loop 140 will adjust the control signal  $V_{\text{tune}}$  for decreasing  
4 the delay of delay element 144 to accommodate the delay increase experienced by delay block  
5 146. However, if the variable delay element 144 is already at the lower end of its adjustable  
6 range, then an increase in delay of delay block 146 will cause the delay lock loop to lose lock  
7 given that a further decrease in the delay of variable delay element 144 is not available.

8 Recognizing these limitations, the circuits and methods disclosed herein provide a  
9 variable delay element 144 of a delay lock loop with the ability to be set to an initialized tune  
10 position of reliable operation.

11 For an exemplary initialization sequence, and referring to Figures 8 and 11, lock  
12 sequencer 168 sends control signal 170 for configuring first switch 150 to couple the input of  
13 variable delay element 144 to the output of divider 142, and a second control signal 172 for  
14 configuring second switch 152 to couple the variable input 153 of the phase detector 154 to  
15 receive the signal from delay block 146. Lock sequencer 168 provides a third control signal that  
16 holds switch 160 closed for coupling the output of charge pump 156 to capacitor 158.

17 Additionally, the divided clock signal of divider 142, can be used to drive a timer (or  
18 counter) within the lock sequencer for advancing the initialization sequence of the delay lock  
19 loop. Alternatively, lock sequencer 168 receives the clock signal directly from input 141.

20 Pursuant to the initialization sequence, at a time  $T_0$ , a reset signal is high and switch 164  
21 closed for coupling control terminal 166 of variable delay element 144 to the  $V_{\text{min}}$  clamping  
22 voltage. The level of  $V_{\text{min}}$  is selected for setting the variable delay element 144 to its minimum  
23 settable delay. Subsequently, at time  $T_1$ , the reset signal transitions low for disconnecting the  
24 control terminal 166 from the clamping voltage  $V_{\text{min}}$ . At this time, phase detector 154, charge  
25 pump 156, and capacitor 158 generate control signal  $V_{\text{tune}}$  to increase the delay of variable delay  
26 element 144. The tune signal continues to ramp until transitions of the variable signal at variable  
27 input 153 move into synchronization with transitions of the reference signal at reference input  
28 155.

29 With divider 142 within the control loop of the delay lock loop during initialization, the  
30 delay lock loop will acquire lock upon the variable delay element slipping the variable signal 153  
31 by a delay sufficient to correlate transitions of that signal to transitions of the reference signal

1 155. For example, assuming a clock input of 500 MHz, and assuming that divider 142 divides  
2 the CLKIN signal by four, the delay of variable delay element 144, when added to the  
3 propagation delay of 146, preferably provides a delay of 8ns, i.e., four times the clock period of  
4 2ns, whereupon transitions of the variable signal 153 will coincide with transitions of the  
5 reference signal 155.

6 At time  $T_2$ , the first switch 150 is configured to channel the input CLKIN signal directly  
7 to the variable delay element 144. In addition, lock sequencer 168 opens switch 160 to  
8 temporarily disconnect capacitor 158 from charge pump 156. Switch 160 is temporarily opened  
9 to prevent any control loop transients resulting from noise of delay lock loop reconfiguration  
10 from impacting stable control of variable delay element 144.

11 At time  $T_3$ , lock sequencer 168 re-configures switch 152 to couple the output of second  
12 divider 148 to the variable input 153 of phase detector 154. Preferably, during the hold time  
13 between times  $T_3$  and  $T_2$ , the input clock signal will have propagated through variable delay  
14 element 144, delay block 146, and divider 148. Next, the lock sequencer closes switch 160 to  
15 couple the output of charge pump 156 to integrating capacitor 158. Using this initialization  
16 sequence, variable delay element 144 is initialized to a mid-region of its adjustable tune range so  
17 that the delay lock loop may reliably operate within the adjustment range of variable delay  
18 element 144 for accommodating delay increases or fluctuations of delay block 156.

19 Variable delay element 144 is initialized to a setting that is above its minimum settable  
20 delay by an amount greater than the anticipated variation of delay block 146 over its anticipated  
21 ambient operating conditions. Accordingly, the divisor N of first divider 142 is selected with a  
22 magnitude to assure that N cycles of the input clock ( $N \cdot T_{\text{clock}}$ ) is greater than the anticipated total  
23 delay of delay block 146 over its anticipated ambient operating conditions.

24 In accordance with an alternative embodiment, further referencing Figure 8, a direct  
25 electrical coupling is provided between the output of delay block 146 and the variable input 153  
26 of phase detector 154. During operation of the delay lock loop, phase detector 154 compares the  
27 variable signal at input 153 to the reference signal at reference input 155. Although, the  
28 frequency of the variable signal is greater than that of the reference signal, meaningful phase  
29 errors can be determined by comparing each transition of the reference signal to every, for  
30 example, 4<sup>th</sup>, 5<sup>th</sup>, 6<sup>th</sup>, etc., transition of the variable signals, depending upon their harmonic  
31 relationship as determined by divisor N. For this alternative embodiment, to assure that

1 transitions of the signal at output 147 are coincident with those at input 141, optional delay unit  
2 174 can be disposed between the destination output 147 and the variable input 143 of phase  
3 detector 154 to provide a delay equal to that of first divider 142.

4 The feedback circuit 162 of the delay lock loop pursuant to the embodiment disclosed in  
5 Figure 8 comprises charge pump 156, switch 160, accumulation capacitor 158 and reset switch  
6 164. However, it is understood that alternative exemplary embodiments of feedback circuit 162  
7 may be comprised of other circuits that are able to effectively integrate the error signal  
8 responsive to the detected phase differences of phase detector 154, hold the generated tune signal  
9  $V_{\text{tune}}$  responsive to the hold signal of sequencer 168, and clear the integrated value of the  
10 generated tune signal  $V_{\text{tune}}$  responsive to a reset signal.

11 Thus far, the delay lock loop has been described as accommodating delay variations of  
12 drivers or shaping circuits to provide a clock signal at an output that is coincident with an input  
13 signal. It is further noted that for the particular exemplary embodiment depicted in Figure 8, it  
14 was assumed that the clock signal ran continuously and that it was always available to the delay  
15 lock loop.

16 In accordance with alternative embodiments of the present invention, a compound delay  
17 lock loop architecture 180 is provided to address synchronous data transfer applications in  
18 situations where a plurality of clock signals is required, each of said clock signals having  
19 selectable timing relative to the others. For example, with reference to Figures 9A and 9B, a  
20 clock signal at input 141 is applied to divider 142 and a first terminal of switch 150. The divider  
21 output is coupled to the second terminal of switch 150 and also to the reference input 155 of  
22 phase detector 154. The output of switch 150 feeds variable delay element 144, preferably, but  
23 optionally, via duty cycle compensator 181. Inner vernier delay lock loop 182 receives the  
24 output of variable delay element 144 and provides a plurality of variously delayed  
25 representations of the received signal at its plurality of output taps  $T_0$  through  $T_n$ . Multiplexer  
26 184 selects, per control select signals applied thereto, optimal phase representations of the clock  
27 signal for use with the associated clocking applications. Further description of inner vernier  
28 delay lock loop 182 and multiplexer 184 and their operation may be found in U.S. patent  
29 application serial no. 08/879,845 filed June 20, 1997, assigned to the assignee of the present  
30 application, and hereby incorporated by reference in its entirety.



1 One output, for example, the first output, of vernier delay lock loop 182 is coupled to  
2 emulator circuit 186. Emulator circuit 186 provides a propagation delay that corresponds to  
3 circuitry of multiplexer 184, and/or associated buffers, switching elements, shaping circuits and  
4 other conditioning circuits. The output of emulator circuit 186 is routed to the variable input 153  
5 of phase detector 154 via divider 148 or delay unit 174, as determined in accordance with the  
6 configuration of switch 152.

7 As before, phase detector 154 provides an error signal responsive to a phase difference  
8 determined between the variable signal at the variable input 153 and the reference signal at the  
9 reference input 155. Charge pump 156 and capacitor 158 integrate the error signal. Capacitor 158  
10 accumulates the charge provided by charge pump 156 to provide the control signal  $V_{\text{tune}}$ . Lock  
11 sequencer 168 is operative to advance the delay lock loop through various configurations of an  
12 initialization sequence so as to initialize the delay lock loop 180 with the variable delay element  
13 144 set to a mid-range of its adjustable range.

14 For example, at start up, and with reference to Figures 9A, 9B and 11, lock sequencer 168  
15 configures first switch 150 for coupling the input of variable delay element 144 to receive the  
16 divided output signal of divider 142, while the second switch 152 is configured for coupling the  
17 output of emulator circuit 186 to the variable input 153 of phase detector 154. At time  $T_1$ , reset  
18 switch 164 is disabled so that capacitor 158 is allowed to accumulate charge as provided by  
19 charge pump 156. Charge pump 156 begins ramping the control signal  $V_{\text{tune}}$  to increase the delay  
20 of variable delay element 144. As this occurs, eventually, transitions of the variable signal at the  
21 variable input 153 of phase detector 154 will coincide with those of the reference signal at  
22 reference input 155. This ramping duration is affected by the value of the divider 142's divisor  
23 N. Similarly, and as discussed with respect to Figure 8, the divisor value is selected such that the  
24 product of N cycles of the input clock, i.e.,  $N \cdot T_{\text{clock}}$  will be greater than the anticipated delay  
25 variation extent of emulator circuit 186.

26 At time  $T_2$ , lock sequencer 168 changes the first control signal to configure switch 150 to  
27 channel the clock input signal 141 to the input of variable delay element 144, which signal path  
28 preferably includes optional duty cycle compensator 181. Next, at time  $T_3$ , the lock sequencer  
29 reconfigures switch 152 for coupling the output of the second divider 148 to the variable input  
30 153 of phase detector 154. In accordance with an alternative aspect of this embodiment, a delay

1 unit 174 is provided between emulator circuit 186 and phase detector 154, and whose function  
2 was explained earlier.

3 During the interval of time between the reconfiguration of the first and second switches  
4 150, 152, i.e., between times  $T_2$  and  $T_3$  respectively, switch 160 is preferably disabled to hold the  
5 value of the control signal  $V_{tune}$ , allowing the undivided clock to propagate through variable  
6 delay element 144, vernier DLL 182, emulator circuit 186, and divider 148 of the delay lock loop  
7 before returning switch 160 to its closed position. This prevents the loop from being disturbed by  
8 the two different frequencies that are transiently present at the inputs of phase detector 154  
9 during reconfiguration of the delay locked loop.

10 A more detailed description of an exemplary compound delay lock loop is provided with  
11 reference to Figure 10. Delay lock loop 180 receives an input clock ClkIn at input 141. Buffer  
12 143 passes the clock to the respective clock inputs of divider-switch-A (142', 150') and divider-  
13 switch-B (148', 152'). (For purposes of simplifying the present description, it will be understood  
14 that reference to a signal may be directed to both its primary and complementary parts. For  
15 example, "clock input" 141 is meant to encompass both its primary input 141A and its  
16 complementary input 141B, which are associated with the respective primary and  
17 complementary clock signals ClkIn and ClkIn\_.) Divider-switch-A (142', 150') which  
18 comprises division circuitry 142' and multiplexer 150', is shown in further detail in Figure 12.  
19 The division circuitry comprises a plurality of D flip-flops serially arranged such that the Q  
20 outputs of flip-flops 190, 192, 194 feed the D inputs of the subsequent flip-flops 192, 194, 196  
21 respectively. These serially configured D flip-flops each have their clock inputs tied to receive  
22 clock signal Clk from the clock input terminal 208. The Q output of flip-flop 196 is inverted by  
23 inverter 198 and is fed back as the D input to flip-flop 190, in what is known in the art as a  
24 "Johnson counter." A selectively configurable switch 206 establishes a programmable divisor  
25 value of divider 142'. With the switch 206 configured in its lowest select position, as shown in  
26 Figure 12, the output of flip-flop 194 would be coupled to the D-input of flip-flop 196 to provide  
27 the divider 142' a divisor value of 8. When switch 206 is configured to select the middle select  
28 terminal, the output of flip-flop 192 feeds the D-input of flip-flop 196 to provide a divisor of 6.  
29 Finally, if switch 206 is configured to select the upper select terminal, the output of flip-flop 190  
30 is coupled to the input of flip-flop 196 and provides a divisor of 4.

Continuing with reference to Figure 12, the reset input 209 allows the divider 142' to be cleared, thereby configuring all flip-flops to a zero state, output condition. The select line 210, corresponding to the control line 170 of Figures 8, 9A, and 9B, allows a controller, e.g. a lock sequencer, to configure multiplexer 150 to select one of either the clock signal or the divided clock signal for output 202, CLKOutA. The output of inverter 198 is passed through inverter 199 to form RefCLK 155, the reference input to phase detector 154. Another buffered output 200 of the first divider 142 provides a signal to the second divider-switch-B (148', 152') for selective use, as will be described more fully subsequently herein, to keep the second divider of the DLL in a known state relative to that of the first divider. The output of selector 206 is coupled to 204, CCLKOut, to provide the appropriate phase of the frequency-divided clock to the counter in the lock sequencer.

Returning to Figure 10, the primary output 202 of first divider switch (142', 150') is fed to variable delay element 144, preferably, by way of duty cycle compensator 181. Duty cycle compensator 181 conditions the signal to assure a 50/50 duty cycle or symmetry for its output signal. However, if the input signal is known to have sufficient symmetry, the duty cycle compensator can be omitted.

Variable delay element 144 provides a propagation delay therethrough that is established in accordance with the value of the control signal  $V_{tune}$ , which is received at its control input 166. The delayed signal that is output from variable delay element 144 is coupled to inner vernier DLL 182. Inner vernier DLL 180 provides a plurality of variously delayed output signals at respective plurality of output taps  $T<0:15>$ . The plurality of output taps  $T<0:15>$  are coupled to multiplexer 184. Multiplexer 184 selects, as determined by the select and control signals 188, the respective optimal signals that are to be used for the various clocking applications within the memory. Such clocking applications may include, for example, latching data into a data input latch, or presenting a clock signal to a synchronous clock output terminal for accompanying data read from the memory.

One output of multiplexer 184, e.g.  $T<0>$ , is coupled to the input of emulator circuit 186' (see Figure 10A). The emulator circuit 186' emulates signal conditioning circuitry that may be associated with, for example, propagating data from a data output latch to a data output terminal. Such conditioning circuits may include, for example, shaping circuits, output buffers, or tri-state buffers disposed in the data path immediately preceding the memory's data output terminals.

1 With the emulator circuit 186' of the delay lock loop providing surrogate emulation of the  
2 conditioning circuits associated with the data output signal path, the control loop of the clock  
3 signal's compound delay lock loop will keep the clock signal as presented at the memory's  
4 output clock terminal in substantially synchronous relationship relative to the data signal  
5 presented to the memory's data output terminals. Accordingly, emulator circuit 186', by  
6 providing a propagation delay therethrough which emulates the data output signal path, enables  
7 the compound delay lock loop to maintain a substantially optimal timing relationship relative to  
8 the memory's data output signal, thereby compensating for timing fluctuations of the above-  
9 mentioned conditioning circuits.

10 The output of emulator circuit 186' is fed forward to divider-switch-B (148', 152'),  
11 which is exemplified in Figure 13. Similar to Figure 12, divider-switch-B includes a divider  
12 portion 148' and multiplexer 152'. Divider 148' is made up of a plurality of serially arranged D-  
13 flip-flops 220, 222, 224, 226. A multi-position switch determines from which of the flip-flops  
14 220, 222, 224 to source the input of flip-flop 226, and, accordingly, provides selective  
15 programmability of the divisor of divider 148' as explained earlier. Inverter 228 feeds the  
16 counter's output signal back to an input of multiplexer 230, which multiplexer selectively  
17 couples, as determined by control signal SelB, one of either the counter's fed-back output signal  
18 or an external synch signal to the D-input of first flip-flop 220. This arrangement is configured  
19 as a shift register during lock sequencing. The output of divider 142' is clocked into the input of  
20 the shift register, so that the outputs of each flip-flop in 148' will match the respective outputs of  
21 the flip-flops in 142'. When SELB selects feedback from inverter 228 at the end of the lock  
22 sequence, the shift register 148' is converted into a Johnson counter which is in lock-step with  
23 Johnson counter 142' of Figure 12, as will be discussed in more detail below.

24 Control signal SelB at input 240, which corresponds to control line 172 of Figures 9A  
25 and 9B, controls the configurations of multiplexers 230, 232 and 152'. In a synchronizing  
26 operation mode, control signal SelB configures multiplexers 230, 232, 152' to couple the Synch  
27 signal 234 to the D-input of flip-flop 220, the ClkIn signal 236 to the clock inputs of the plurality  
28 of flip-flops, and the delayed clock signal, Delayed ClkIn through the optional delay unit 174 to  
29 output 153. For this synchronizing operation mode, as used during a portion of the initialization  
30 of the delay lock loop, the states of divider 148' are kept correlated to those of the first divider  
31 142' in order to assure a stable continuity in the operation of the delay lock loop through one of

1 its reconfiguration transitions, for example, when coupling the output of second divider 148' to  
2 the variable input 153 of the delay lock loop's phase detector 154. During this reconfiguration,  
3 control signal SelB sets multiplexers 230, 232 to couple the counter's fed-back output signal to  
4 the D-input of flip-flop 220, and to couple the delayed clock signal of input 238 to the clock  
5 inputs of the plurality of flip-flops respectively.

6 Absent the synchronizing operation mode of divider 148', state transitions of the divided  
7 variable signal at variable input 153 of phase detector 154 might otherwise be non-coincident  
8 with the transitions of the reference signal at reference input 155 at the time the delay lock loop  
9 is reconfigured. Accordingly, the delay lock loop might have to re-seek a synchronous locked  
10 state. Although the delay lock loop might eventually re-acquire lock, the re-acquisition process  
11 could introduce undesirable transients or noise into the control loop during operation of the delay  
12 lock loop, and accordingly extend the amount of time required for its initialization.

13 Accordingly, for the preferred, yet optional, present embodiment of the invention, and  
14 returning to Figure 10, buffers 143 supply the input clock signal to divider-switch-B (148', 152')  
15 which corresponds to clock input 236 of Figure 13. Furthermore, divider-switch-A (142', 150')  
16 of Figure 10 supplies a synch output signal to be coupled to the synch input of divider-switch-B  
17 (148', 152') (i.e., the synch input 234 of Fig. 13) to facilitate pre-alignment of divider 148'  
18 during a segment of the delay lock loop's initialization.

19 Again, the output of divider-switch-B (148', 152') corresponds to variable input 153 of  
20 phase detector 154. Phase detector and charge pump 154, 156 receive the reference and variable  
21 input signals and output charge responsive to the phase differences determined therebetween.  
22 Exemplary phase detector and charge pump circuits 154, 156 are disclosed in U.S. patent  
23 application serial number 09/260,216, filed January 3, 1999, which is owned by the assignee of  
24 the present application, and which is hereby incorporated by reference in its entirety. For  
25 purposes of developing a better understanding of certain aspects of the present invention, a few  
26 exemplary elements of a phase detector and charge pump are described below with reference to  
27 Figures 14-17.

28 Referring to Figure 14, phase detector 154 comprises a first channel 154A and a second  
29 channel 154B. The circuit of the first channel 154A receives four inputs, a variable complement  
30 signal V\_, primary reference signal R, and control signals SETA\_ and RSTA\_. The control  
31 signals SETA\_ and RSTA\_ control set and reset operations of the first channel 154A of the

1 phase detector. The second channel 154B of the phase detector corresponds to the first channel,  
2 with the exception that the input signals are the primary variable signal V, the reference  
3 complement signal R\_, and control signals SETB\_ and RSTB\_.

4 Moving forward with reference to Figure 15, the first channel 154A of the phase detector  
5 comprises first and second pulse generating circuits 310, 320 respectively. Pulse generator circuit  
6 310 comprises inverters 312A, 314A, 315A, 316A, NAND gate 313A, and NAND gate 318A.  
7 The variable complement signal V\_ is coupled to the input of inverter 312A which inverter feeds  
8 a first input of NAND-gate 313A. The second input of NAND-gate 313A is coupled to receive  
9 the first control signal SETA\_. The output of NAND-gate 313A drives the serial path comprising  
10 inverters 314A, 315A, 316A to a first input of NAND-gate 318A. The other input of NAND-gate  
11 318A receives the variable complement signal V\_ directly. For the following discussion, assume  
12 that SETA\_ and RSTA\_ are held at a logic "1" level.

13 In operation, when the variable complement signal V\_ has been at logic 0 for an extended  
14 period of time, the steady-state condition of the pulse generator 310 will place the output of  
15 inverter 316A in a logic 1 level, which is presented to the first input of NAND gate 313A. With a  
16 logic 0 at the second input of NAND-gate 318A, the output of NAND-gate 318A is high. In  
17 dynamic operation, when the variable complement signal V\_ transitions from 0 to 1, the new  
18 logic 1 level is presented to the second input of NAND-gate 318A while the low-to-high  
19 transition propagates through inverter 312A, NAND-gate 313A, and inverters 314A, 316A.  
20 During the period of time required for propagating the transition through the inverters and  
21 NAND-gate devices, both inputs of the NAND-gate are high so as to provide a logic 0 level at  
22 the output of NAND-gate 318A. Once the transition has propagated through the inverter devices,  
23 the first input of NAND-gate 318A will transition low, for returning the output of NAND gate  
24 318A to a logic 1 level and completing the duration of the logic 0 level pulse.

25 The output of the pulse generating circuit 310 (i.e. the output of NAND-gate 318A) is  
26 coupled to a first input of 3-input-NAND-gate 352. NAND-gate 352 is configured in  
27 combination with NAND-gate 354 to provide a latch circuit, wherein the output of NAND-gate  
28 352 is coupled to one of the inputs of NAND-gate 354, and wherein an output of NAND-gate  
29 354 is coupled back to one of the inputs of NAND-gate 352. When pulse circuit 310 transitions  
30 from high to low, the low signal received at the first input of NAND-gate 352 will drive the  
31 output of NAND-gate 352 into a logic I level, which in turn drives an input of NAND-gate 354.

1 Assuming other inputs of NAND-gate 354 are held high, the output of NAND-gate 354 will  
2 transition from high to low. Accordingly, latch 350 latches a logic 1 level at the output of  
3 NAND-gate 352, and a logic 0 level at the output of NAND-gate 354.

4 NAND gates 365 and 366 buffer the Q and Q<sub>̄</sub> outputs of flip-flop or latch 350 to the  
5 output terminals 306 and 307 for supplying signals QA and QA<sub>̄</sub>. Inverters 361, 362 forward the  
6 output of NAND-gate 318A to an input of NAND-gate 366 and operate to expedite a transition  
7 of the output signal QA<sub>̄</sub> in response to a pulse of pulse generator 310.

8 For the previously described operation of pulse generator 310, it was assumed that the  
9 control signals SETA<sub>̄</sub> and RSTA<sub>̄</sub> were held at logic "1" during its normal operation.  
10 Accordingly, NAND-gates 313A and 318A functioned as inverters. However, either one of the  
11 control signals SETA<sub>̄</sub> or RSTA<sub>̄</sub> can be held low to provide a set or reset, respectively, of latch  
12 350.

13 Pulse generator 320, like pulse generator 310, is configured to be responsive to a  
14 transition of reference signal R to produce a low pulse at the output of NAND-gate 318B with a  
15 pulse duration corresponding to the combined propagation delay of inverter 312B, NAND-gate  
16 313B, and inverters 314B, 315B, 316B. Additionally, inverters 363, 364 propagate the output of  
17 NAND-gate 318B to an input of NAND-gate 365 to expedite a transition of the QA<sub>̄</sub> signal at  
18 output 306 responsive to pulse generator 320.

19 The second channel 154B of the phase detector operates similarly to the first channel  
20 154A, but employs primary variable signal V and reference complement signal R<sub>̄</sub>. To  
21 distinguish the outputs of the first and second channels, outputs 306, 307 of the first channel  
22 154A are annotated to carry complementary signals QA and QA<sub>̄</sub>, while the outputs 308, 309 of  
23 the second channel 154B are annotated to carry complementary signals QB and QB<sub>̄</sub>.

24 The timing diagrams of Figures 16A, 16B and 16C characterize operation of the phase  
25 detector under three conditions. In a first condition, referencing Figure 16A, variable signal V is  
26 phase coherent with reference signal R, and the phase detector's output signal QB corresponds to  
27 a complement of the phase detector's second output signal QA. Under this condition, charge  
28 pump 156 of Figure 14 (which will be addressed in detail with reference to Figure 17) provides  
29 zero output current (I<sub>out</sub>).

30 In a second operating condition, referencing Figure 16B, the phase detector receives a  
31 reference signal R which lags the variable signal by a given phase lag  $\Phi_{lag}$ . Under this phase lag

1 relationship, the output signals QA and QB have overlapping low states that correspond to the  
2 phase lag between the variable and reference signals. During these overlapping low states,  
3 charge pump 156 will respond with a positive output current ( $I^+$ ).

4 Finally, when the phase of reference signal R leads that of variable signal V by a phase  
5 lead  $\Phi_{\text{lead}}$ , the phase detector's output signals QA and QB will have overlapping high states, as  
6 shown in Figure 16C. During these periods of overlapping high states, charge pump 156 will  
7 respond with a negative output current ( $I^-$ ).

8 A particular exemplary embodiment of charge pump 156, referencing Figure 17, receives  
9 four signals at inputs 306, 307, 308, 309, which correspond to the QA, QA\_, QB, and QB\_  
10 output signals from the first and second channels of phase detector 154 of Figure 14. Bias control  
11 signals 474 bias the charge pump by establishing current levels for current sources 470 and 472.  
12 P-channel MOSFET 442 has its source coupled to current source 470, and its drain coupled to  
13 the source of P-channel MOSFET 444. The drain of P-channel MOSFET 444 is coupled to the  
14 drain of N-channel MOSFET 450 at the charge pump's output 460. The source of MOSFET 450  
15 is coupled to the drain of N-channel MOSFET 452, which has its source coupled to current  
16 source 472.

17 During operation of the charge pump, the signal QA at input 306 drives the gates of  
18 MOSFETs 442 and 452, while the signal QB at input terminal 308 drives the gates of MOSFETs  
19 444 and 450. When the signal QA is high, P channel MOSFET 442 is disabled and N-channel  
20 MOSFET 452 is enabled. Additionally, if signal QB is high, then N-channel MOSFET 450 is  
21 enabled and MOSFET 444 disabled. Accordingly, the charge pump 156 may sink a current  
22 through N-channel MOSFETs 450, 452 of a magnitude equal to the current established by  
23 current source 472. Alternatively, if QA and QB are both low, then MOSFETs 442, 444 are  
24 enabled and MOSFETs 450, 452 disabled so that the charge pump may provide an output current  
25 at terminal 460 of a magnitude equal to the current established by current source 470. Finally,  
26 when the input signals QA and QB are not equal, the charge pump neither sinks nor sources an  
27 output current at terminal 460. Further description of this exemplary charge pump 156 and its  
28 associated operation may be found in U.S. patent application serial number 09/260,212, filed  
29 March 1, 1999, assigned to the assignee of the present application and hereby incorporated by  
30 reference in its entirety.



1 Referring again to Figure 10, the output of charge pump 156 is coupled, via switch 160,  
2 to capacitor 158. Capacitor 158 integrates the current provided by charge pump 156 to establish  
3 an accumulation of charge (and associated voltage) that is related to the polarity, magnitude and  
4 duration of the charge pump's current output. Accordingly, the control voltage  $V_{tunc}$  at terminal  
5 166 will ramp up or down dependent upon the polarity of the charge pump's output current.  
6 Again, as addressed previously herein, the control voltage  $V_{tunc}$  at control terminal 166 adjusts  
7 the amount of delay provided by variable delay element 144.

8 To initialize a delay lock loop in accordance with an exemplary initialization sequence of  
9 the present invention, a lock sequencer 168 generates a plurality of carefully timed control  
10 signals for effecting various configurations and reconfigurations of the delay lock loop.  
11 Referring to Figures 18A-C, an exemplary lock sequencer 168 comprises counter 510, which is  
12 shown in detail in Figure 18A. In accordance with a preferred embodiment, counter 510 is a 7 bit  
13 counter configured to receive a clock signal and a reset signal. When operating, counter 510 may  
14 receive a reset signal for clearing its primary outputs  $Q_{<0:6>}$ . Thereafter, and using circuitry  
15 well known in the art, each leading-edge transition of the received clock will increment the  
16 counter through a known binary sequence until the 7<sup>th</sup> bit has transitioned high. Likewise, the  
17 complementary bits  $Q_{<0:6>}$  will follow the complement sequence.

18 It is noted that the counter 510 receives its input clock CCLK from output 204 of divider-  
19 switch-A (see Figs. 10 and 12). Accordingly, each period of the counter's received clock  
20 corresponds to two, four, or six multiple periods of the delay lock loop's input clock signal  
21 CLKIN, wherein the multiple is determined by the divisor of divider 142'.

22 Further referencing Figure 18B, logic circuitry 544 receives six complement output  
23 signals  $Q_{<0:5>}$  from counter 510. So long as one of the six signals  $Q_{<0:5>}$  is high, the output  
24 of logic circuit 544 will be high. The output of logic circuitry 544 feeds an input of latching  
25 NAND-gates 546, 548. The output of NAND-gate 548 drives the D-input of D-flip-flop 550. The  
26 Q output of D-flip-flop 550 provides terminal 552 the LockD control signal for configuring the  
27 delay lock loop's second switch 152 as discussed previously with respect to Figures 8, 9A, 9B,  
28 and 10. After a counter reset, the  $Q_{<0:5>}$  bits of counter 510 are high and the control signal at  
29 terminal 552 will transition to a logic 0 level upon D-flip-flop 550 receiving the next CLKIN  
30 edge. This control signal will remain low until all  $Q_{<0:5>}$  bits of the counter have transitioned  
31 low and another CLKIN edge has been received by flip-flop 550.

1 Referring to Figure 18C, NAND-gate 536, latching NAND-gates 538, 540 and flip-flop  
2 542 are configured to provide a Lock control signal at terminal 543 responsive to the counter's  
3 output signals  $Q_{<2:5>}$ . The output of NAND-gate 536 feeds an input of latching NAND-gates  
4 538, 540. The other input of the latching NAND gates is coupled to receive the reset signal  
5  $RST_{\overline{}}$ . The output of NAND-gate 540 drives the D-input of D-flip-flop 542, which flip-flop  
6 provides the Lock control signal for controlling the configuration of the first switch 150 of the  
7 delay lock loop, as discussed previously with respect to Figures 8, 9A, 9B, 10 and 12. When the  
8 counter is reset, the signals  $Q_{<2:5>}$  are all low to effect a logic 1 level at the output of NAND-  
9 gate 536. When signals  $Q_{<2:5>}$  all go high, the output of NAND-gate 536 will go low. Latch  
10 538, 540 receives the logic 0 level and responds by presenting a logic 0 level to the D-input of  
11 flip flop 542. Accordingly, upon receipt of the next CLKIN edge, the flip-flop transitions the  
12 Lock control signal to a logic 0 level.

13 NAND-gate 536 also drives an input of three other NAND-gates 520, 522, and 524,  
14 which are associated with generating the control signals  $SETB_{\overline{}}$ ,  $RSTA_{\overline{}}$  and  $RSTB_{\overline{}}$   
15 respectively. As discussed previously with respect to Figures 10 and 14-17, these set and reset  
16 signals can be used to control various operations of the circuits of the delay lock loop, including  
17 phase detector 154 and charge pump 156. Again, when the counter receives a reset, it advances  
18 its count until eventually all of the  $Q_{<2:5>}$  bits are high and the output of NAND-gate 536  
19 transitions low. For one cycle of CCLK, the output of NAND-gate 536 remains low. But once  
20 the counter's 7<sup>th</sup> complement bit  $Q_{\overline{<6>}}$  transitions low, the counter's count sequence is  
21 complete, and the counter will provide logic 0 levels for the  $Q_{<2:5>}$  bits such that the output of  
22 NAND-gate 536 returns to a logic 1 level.

23 Further referencing Figure 18C, NAND-gate 512 comprises five inputs that are coupled  
24 to respective complement outputs  $Q_{\overline{<2:6>}}$  of counter 510. The output of NAND-gate 512 drives  
25 the D-input of flip-flop 514, which flip-flop sources a control signal  $PInit_{\overline{}}$  at terminal 516. The  
26  $PInit_{\overline{}}$  control signal of flip-flop 514 also drives an input of NAND-gate 524 associated with the  
27  $RSTB_{\overline{}}$  control signal, an input of NAND-gate 520 associated with the  $SETB_{\overline{}}$  control signal,  
28 and, additionally, the reset terminals of D-flip-flops 556 and 554. When the  $Q_{\overline{<2:6>}}$   
29 complement bits of counter 510 all transition high following a counter reset, NAND-gate 512  
30 presents a logic 0 level to the input of D-flip-flop 514. The output of D-flip-flop 514,  
31 accordingly, will remain low with each CCLK transition until the  $RST_{\overline{}}$  signal has cleared and

the 3<sup>rd</sup> complement bit Q<sub>(2)</sub> of the counter has transitioned low; whereupon, the flip-flop 514 captures and outputs a logic 1 level upon receipt of the next CCLK edge.

**TABLE 1**

	Q6	Q5	Q4	Q3	Q2	Q1	Q0
0T	0	0	0	0	0	0	0
1T	0	0	0	0	0	0	1
2T	0	0	0	0	0	1	0
4T	0	0	0	0	1	0	0
8T	0	0	0	1	0	0	0
16T	0	0	1	0	0	0	0
32T	0	1	0	0	0	0	0
64T	1	0	0	0	0	0	0

A description through an exemplary counter sequence now follows with reference to the schematic of Figure 18 and Table 1. At start-up, the reset signal RST transitions high, and, likewise, its counterpart complement reset signal RST<sub>̅</sub> transitions low. The primary outputs Q<0:6> of counter 510 are set low, while the complement outputs Q<sub>̅</sub><0:6> are set high. Responsive to the counter reset and the complement reset signal RST<sub>̅</sub>, latching NAND-gates 546, 548 output a logic 0 level at the output of NAND-gate 548, the control signal Phold<sub>̅</sub> at the output of NAND-gate 536 transitions high, and latching NAND-gates 538, 540 output a logic 0 level at the output of NAND-gate 540. Additionally, flip-flop 514, responsive to the complement reset signal RST<sub>̅</sub> at its active low set input, outputs a logic 1 level while receiving at its input a logic 0 level from NAND-gate 512. Under these setup conditions, D flip-flops 514, 550 and 542 are presented with logic 0 levels at their D inputs and in a condition for latching and outputting logic 0 level output signals upon receipt of each flip-flop's respective next clock

1 transition. The lock sequencer 168 is configured to begin the initialization sequence for setting  
2 the delay lock loop into a stable operating position.

3 Referencing Table 1, following a first CCLK period 1T after the reset, the counter's least  
4 significant bit Q0 transitions high and its complement counterpart  $\overline{Q_0}$  transitions low. Logic  
5 circuit 544 maintains a same level as presented to latching NAND-gates 546, 548, and control  
6 signal Phold\_ at the output of NAND-gate 536 remains the same as presented to latching NAND-  
7 gates 538, 540. However, the outputs 552, 543 of respective D-flip-flops 550, 542 transition low  
8 for effecting low state transitions of the LockD and Lock control signals respectively.  
9 Accordingly, first switch 150 of the delay lock loop, (see Figs. 8, 9A, 9B, 10) is configured to  
10 couple the divided signal to variable delay element 144, and second switch 152 is configured to  
11 couple variable input 153 of phase detector 154 to receive its signal from emulator block 146 or  
12 186.

13 Additionally, flip-flop 514 transitions the PInit\_ control signal low, which will cause the  
14 outputs of NAND-gates 520 and 524 to transition high. As a result, control signal  
15 SETB\_ transitions low via inverter 526 and control signal RSTB\_ transitions high. The low  
16 PInit\_ control signal will also reset flip-flops 554 and 556. The low output from flip-flop 556  
17 will feed NAND-gate 522 to effect a logic 0 level for control signal RSTA\_ at output 532 via  
18 inverter 528. With control signals SETB\_ and RSTA\_ both low, the first and second channels of  
19 phase detector 154 (see Figs. 15 and 17) will provide the QA and QB output signals at logic 0  
20 and logic 1 levels respectively. Therefore, charge pump 156 (see Fig. 17) will have its output  
21 configured in a tri-state condition, with P-channel MOSFET 444 and N-channel MOSFET 452  
22 both disabled. With output 460 of charge pump 156 in a tri-state condition, exemplary clamp  
23 circuit 164 (see Figs. 10 and 19) can be enabled to supply the integrating capacitor 158 a bias  
24 voltage from bias circuit 605. To enable the clamp circuit, the logic 0 level of control signal PInit  
25 configures multiplexer 604 to couple the output voltage of bias circuit 605 to output 610.  
26 Accordingly, integrating capacitor 158 will be charged with the output voltage level of bias  
27 circuit 605, which level is previously selected to adjust variable delay element 144 to its lower  
28 delay setting.

29 Continuing the count sequence, and further referencing Table 1, after three more CCLK  
30 cycles, at time 4T, output Q2 of the counter 510 becomes a logic 1 and its complement output  
31  $\overline{Q_2}$  becomes a logic 0. In response, the output of NAND-gate 512 will transition high, whereby

1 D-flip-flop 514 will transition the PInit\_ control signal high at the next CCLK transition (at time  
2 5T). Once the PInit\_ control signal transitions high, the control signals SETB\_ and RSTB\_ take  
3 on high and low values respectively.

4 Regarding control signal RSTA\_, flip-flop 556 maintains a logic 0 level at its output to  
5 NAND-gate 522 so long as transitions of the variable signal V lag those of the reference signal R  
6 by less than 180 degrees. However, beyond time 5T, once an upward transition of the variable  
7 signal V at the D-input of flip-flop 554 lags an upward transition of the reference signal R at the  
8 clock input of flip-flop 554 by more than 180 degrees, flip-flop 554 will then capture a high  
9 value for sending a transition to the clock input of flip flop 556. Accordingly, flip-flop 556 will  
10 capture a logic 1 level for output to NAND-gate 522. In other words, while the variable signal  
11 lags the reference signal by less than 180 degrees, phase detector 154 will output logic 0 levels  
12 for the QA and QB signals that are provided to charge pump 156 (see Figs. 15 and 17) and  
13 charge pump 156 will output a positive current  $I^+$  of a magnitude corresponding to that of current  
14 source 470. It is understood that the current source 470 will have been re-enabled responsive to  
15 the PInit control signal returning to its logic 1 level. With charge pump 156 providing positive  
16 output current, capacitor 158 accumulates charge for ramping the control signal  $V_{tune}$  upwardly  
17 to increase the delay of variable delay element 144. Increasing the delay of variable delay  
18 element 144, in turn, delays the variable signal V relative to the reference signal R at flip-flop  
19 554. The integration of the output current and ramping of the control signal  $V_{tune}$  continue until a  
20 sufficient phase lag has been introduced to the variable signal V by variable delay element 144 to  
21 enable a rising transition of the reference signal R to capture a logic 1 level of the variable signal  
22 V.

23 Once the variable signal V has been sufficiently delayed, the D-flip-flop 554 latches a  
24 logic 1 level for output to the clock input of D-flip-flop 556. Again, as discussed previously, flip-  
25 flop 556 (which has its D-input held high) receives the logic 1 level transition at its clock input  
26 and captures the logic 1 state for output to NAND-gate 522, while the complement output  $Q_-$  of  
27 flip-flop 556 is coupled to an input of NAND-gate 524. Once the control signals RSTA\_ and  
28 RSTB\_ have both transitioned high, normal operation of the delay lock loop's phase detector and  
29 charge pump 154, 156 ensues. In this fashion, the phase detector and charge pump 154,156  
30 provide an upward ramping of the control signal  $V_{tune}$  for adjusting variable delay element 144  
31 away from its previously clamped, minimum delay setting. Feedback will now cause the delay

1 to continue to increase until V lags R by 360 degrees. Without this initialization sequence, the  
2 loop would have attempted to lock at zero degrees, which is impossible.

3 At time 32T, the counter's sixth bit Q<sub>5</sub> transitions high and its corresponding  
4 complement bit Q<sub>5</sub> transitions low. Eventually, at time 60T, all the inputs of NAND-gate 536  
5 are high, and its output transitions low. Accordingly, the D-input of flip-flop 542 is presented a  
6 logic 1 level and the control signals SETB\_ and RSTA\_ at terminals 530, 532 respectively, both  
7 transition low. In response to this transition, phase detector 154 (see Fig. 15) provides logic 0  
8 and logic 1 levels for the respective QA and QB output signals, thereby configuring the output  
9 460 of charge pump 156 into a tri-state condition. With the output of charge pump 156 disabled,  
10 capacitor 158 will hold the voltage level of control signal V<sub>tune</sub>. Thus, the tri-state operability of  
11 charge pump 156 has been likened to switch 160 as was previously discussed with respect to  
12 Figures 8, 9A and 9B. However, for a preferred embodiment, the functionality of switch 160 is  
13 understood to be provided by the tri-state operability of charge pump 156.

14 After another CLKIN edge, at time 60T<sup>+</sup>, D-flip-flop 542 provides a logic 1 level for  
15 control signal Lock at terminal 543 which will configure the first switch 150 (see Figs. 8-10) to  
16 couple the input clock signal directly to variable delay element 144. Next, at time 63T, all six  
17 bits Q<sub><0:5></sub> will be low at the input of logic circuit 544, so that D-flip-flop 550 will provide a  
18 logic 1 level for the control signal LockD at terminal 552 upon receipt of the next clock edge at  
19 time 63T<sup>+</sup>. Accordingly, the second switch 152 is configured to couple the output of second  
20 divider 148 to the variable input 143 of phase detector 154. It will be noted that the SETB\_ and  
21 RSTA\_ control signals are held low during this transition interval to keep the output of charge  
22 pump 156 in a tri-state condition to preserve the value of the control signal V<sub>tune</sub> at capacitor 158  
23 while the other signals of the newly reconfigured delay lock loop stabilize.

24 In accordance with this embodiment, and referring to the timing diagram of Figure 11, a  
25 delay is provided between the upward transition of the control signal Lock at terminal 543  
26 relative to the upward transition of the control signal LockD at terminal 552. By providing such a  
27 delay before reconfiguring the second switch 152, the new input signal propagates through  
28 variable delay element 140, emulator circuit 146 and second divider 148 (see Figs. 8, 9A, 9B)  
29 before the second switch couples the resultant signal to the phase detector. Accordingly, and  
30 again, pursuant the present disclosure, the control loop is protected from signal transients that  
31 may be associated with the delay lock loop's reconfiguration. In addition, the second divider can

1 be optimally preset in order to provide output transitions to the phase detector that are  
2 substantially synchronous relative to those which would otherwise have been presented to the  
3 phase detector before the delay lock loop's reconfiguration.

4 Nearing the conclusion of the counter sequence, when the 7<sup>th</sup> bit, Q<sub>6</sub>, of counter 510  
5 transitions high at time 64T, the low complement bit Q<sub>6</sub> is fed back to the counter's input for  
6 signaling a conclusion of the counter sequence. Likewise, pursuant the binary sequence, the  
7 remaining bits Q<sub><0:5></sub> transition low, while the complement bits Q<sub><0:5></sub> transition high. In  
8 response, NAND-gate 536 will transition high, and the control signals SETB<sub>-</sub> and RSTA<sub>-</sub> will  
9 also transition high for beginning normal operation of the delay lock loop with its variable delay  
10 element initialized to a middle region of its adjustable range. With the variable delay element  
11 initialized in this fashion, the delay lock loop can reliably compensate for delay fluctuations of  
12 emulator block 186, vernier delay lock loop 182, and associated multiplexer 184 by adjustment  
13 of variable delay element 144 given that the variable delay element has been initialized away  
14 from its lower limit.

15 For the exemplary lock sequencer 168 described above with reference to Figure 18,  
16 various delays and pulse durations were realized using particular combinations of the counter's  
17 output bits in order to establish a variety of control signals and durations for driving the  
18 initialization of the delay lock loop. It will be understood, that alternative delays and control  
19 signal durations could be provided via other combinations of the counter bits and clock  
20 frequency, or by using other known state machines to sequence the configurations of the delay  
21 lock loop through the initialization sequence of the present invention.

22 In accordance with a further exemplary embodiment, and referring to Figure 20, a  
23 synchronous memory device 610 includes data path subsystem 100 for interfacing memory array  
24 56 with bus 212 to exchange data therebetween. Known command and decode circuitry interpret  
25 command and address information that is received from the bus. Command decoder and  
26 sequencer 82, upon determining a valid command for the memory device, enables decode circuit  
27 84 to decode an address associated with accessing the memory array 56.

28 When receiving command data within command register 66 of the synchronous memory  
29 device 610, clock circuit 86 receives a system clock from clock bus 26 via line 40 and provides  
30 command register 66 an internal clock signal ICLK that is appropriately timed for capturing and  
31 latching command data. Clock circuit 86 preferably comprises a delay lock loop of a previously

1 described exemplary embodiment of the present invention, e.g., a compound delay lock loop as  
2 previously described herein with respect to Figures 9A and 9B. The delay lock loop is configured  
3 to source internal clock signal ICLK as an optimally delayed representation of the system clock  
4 such that transitions of ICLK are synchronous with, and relative to, centers of the data eyes of  
5 the command data signal received at command register 66. Emulator circuitry 186 of such delay  
6 lock loop, preferably emulates circuitry (e.g., multiplexer 184 and associated drivers) involved in  
7 propagating ICLK to command register 66.

8 Further referencing Figure 20, data path subsystem 100 of synchronous memory 610  
9 comprises write channel 112 and read channel 110. Write channel 112 includes receivers 130  
10 which are coupled to receive data from data bus 24 of synchronous bus 212 by way of lines 38B  
11 and data port 39B. Vernier select circuit 136 receives the reference clock that accompanies the  
12 write data from clock bus 26 of synchronous bus 212 by way of line 46 and clock port 45. Given  
13 that the reference clock that accompanies the write data may be discontinuously supplied by  
14 clock bus 26 for brief durations that only cover the data transfer, the configuration of vernier  
15 select circuit 136 is provided a "slaved" vernier design similar to the exemplary block diagram of  
16 Figure 5. In other words, the vernier delay portion 48 of "slaved" vernier select circuit 136 is  
17 controlled by way of a control signal  $V_{\text{tuneA}}$  that has been generated by an inner delay lock loop  
18 of a remote compound delay lock loop for adjusting a separate, but similarly designed vernier.  
19 Referencing Figure 21, vernier delay lock loop 182 incorporates an inner delay lock loop (see the  
20 description presented earlier with respect to Figure 6) as part of the compound delay lock loop  
21 that provides the internal clock ICLK for latching the command data into command register 66.  
22 It is this inner delay lock loop of vernier 182 that provides the control signal  $V_{\text{tuneA}}$  for adjusting  
23 the vernier 48 of "slaved" vernier select circuit 136. Accordingly, vernier 48 of vernier select  
24 circuit 136 is slaved per the control signal  $V_{\text{tuneA}}$  of vernier 182.

25 Additionally, in a preferred, yet optional aspect of the present embodiment, a variable  
26 delay element 144' is disposed in the signal path of the data reference clock that precedes vernier  
27 48, and comprises a circuit design substantially similar to that of variable delay element 144 of  
28 the remote compound delay lock loop. Variable delay element 144' receives a control signal  
29  $V_{\text{tuneB}}$  from the control loop of the outer delay lock loop of the compound architecture. Emulator  
30 circuit 186 of the remote compound delay lock loop, by emulating delays of the drivers and  
31 multiplexer 184 associated with the internal clock signal ICLK, likewise substantially emulates



1 characteristics of similarly designed drivers and multiplexer 52 associated with propagating the  
2 data reference clock signal DCLKD to the clock input of the data registers 132. Accordingly, the  
3 control signal  $V_{tuneB}$  that is used for adjusting variable delay element 144 of the compound delay  
4 lock loop will be substantially suitable for adjusting the delay of the variable delay element 144'  
5 of the vernier select circuit 136. In this fashion, transitions of the discontinuous data reference  
6 clock are maintained in synchronous, relative relationship to the data signal, and the clock  
7 transitions are kept substantially aligned to data eyes of the data signal at the data input of data  
8 register 132.

9 In accordance with an alternative embodiment of the present invention, the clock signal  
10 that accompanies the data signal may be continuous. For such memory applications which have a  
11 continuous write clock accompanying the write data, the vernier select circuit comprises a  
12 compound delay lock loop, e.g., of one of the previously described exemplary embodiments  
13 separate and independent of the delay lock loop that may be associated with receiving the  
14 command data.

15 Further referencing Figure 21, the compound delay lock loop is preferably initialized in  
16 accordance with one of the previously described, exemplary initialization sequences of the  
17 present invention, so that the variable delay element 144 is set to a middle region of its adjustable  
18 range. Accordingly, the delay lock loop can adjust the delay of the variable delay element 144  
19 for accommodating increased delay fluctuations of any drivers and multiplexer 184 associated  
20 with propagating the selected clock signal to the latching registers. Additionally, vernier select  
21 circuit 136 preferably includes an additional output tap 137 configurable to select an optimally  
22 delayed representation of the received write clock for use in transferring and capturing data from  
23 the input registers 132 to the memory's Write Latch and Driver circuit 134. This additional  
24 output tap 137 of the vernier select circuit 136 can comprise a separate programmable channel of  
25 multiplexer 52.

26 Turning to the read data channel 110 of synchronous memory 610, with further reference  
27 to Figure 20, address and decode circuit 84 provides address information to access circuitry 54  
28 for obtaining data from memory array 56. This data is transferred into read latch 120, for  
29 example, as a 64 bit wide data-word. Read latch 120 presents the data to read FIFO circuit 124  
30 by way of time division multiplexer 122, which multiplexer enables time division multiplexing  
31 of the data of latch 120 into four, serially presented, 16-bit data-words. Read FIFO circuit 124

1 sends this multiplexed data out, as clocked by read clock RCLK, to synchronous bus 212 via  
2 drivers 128, port 39B and data lines 38B. Likewise, a reference read clock is also sent to the  
3 synchronous bus 212 via drivers 128 to accompany the data transfer. Ideally, the clock  
4 transitions at the clock output terminal 48 coincide with those of the data signal at data output  
5 port 39B.

6 To facilitate and maintain synchronization between these signals, a delay lock loop  
7 corresponding to one of the exemplary embodiments of the present invention described earlier  
8 herein, e.g., relative to Figures 9A and 9B, is incorporated within a clock vernier portion of Read  
9 FIFO circuit 124. For this particular exemplary embodiment, the emulator circuit 186 of such  
10 compound delay lock loop is designed to simulate delays of the delay lock loop's multiplexer  
11 184, the tri-state or other buffers associated with the delay lock loop's multiplexer 184, and  
12 drivers 128 of the read channel associated with propagating the data to the output port 39B.  
13 Additionally, it will be understood that the output drivers 128 may include conditioning circuits  
14 for shaping the data and clock signals prior their presentation to respective ports 39B, 45. In  
15 operation, initialization of the compound delay lock loop associated with the read clock will  
16 initialize the variable delay element 144 of the delay lock loop for setting it within a middle  
17 region of its operating range as set forth earlier herein. Accordingly, an increase in delay through  
18 the delay lock loop's buffers and multiplexer 184, the buffers of read FIFO circuit 124, and  
19 drivers 128 of the read channel over their ambient operating conditions, can be compensated by  
20 decreasing the delay of the delay lock loop's variable delay element 144.

21 Additional disclosure of the read and write channels 110 and 112 can be found in US  
22 application serial number 08/879,847 filed June 20, 1997, which is hereby incorporated by  
23 reference in its entirety.

24 In accordance with another embodiment of the present invention, referencing Figure 22, a  
25 processing system 600 comprises a processor 602 coupled to a synchronous communication bus  
26 or network 612 that transfers data in synchronous relationship with associated write or read  
27 reference clock signals. The processing system will typically include I/O devices 614, e.g., such  
28 as a keypad and mouse, that are coupled to the bus by way of known, industry standard  
29 interconnect architectures. These I/O devices 614 allow an operator to interact with the  
30 processor system 600. Additionally, the processor system further comprises one or more output  
31 devices 616, such as a printer or video display, that are coupled to the bus using available bridge

1 or expansion bus interfacing architectures. Synchronous memory devices 610A, 610B comprise  
2 one of the previously disclosed, exemplary synchronous memory embodiments of the present  
3 invention, and are configured to exchange data in synchronous relationship with associated read  
4 and write clock signals across bus 612. In operation, processor 602 exchanges data with  
5 synchronous memory devices 610A, 610B per the circuitry and methods disclosed previously  
6 herein relative to Figures 20 and 21. Sustaining the synchronization needs of the processor  
7 system, memory devices 610A, 610B incorporate the exemplary delay lock loops and  
8 initialization circuits disclosed previously. Such initialization and synchronization circuits can  
9 configure the memory to maintainable settings within the processor system 600 for providing  
10 reliable synchronous data transfer capabilities within the processor system over its ambient  
11 operating conditions.  
12  
13